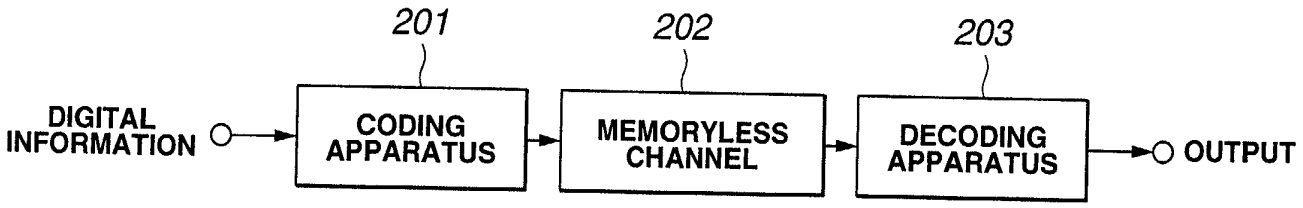
201
202
203
DIGITAL INFORMATION
CODING APPARATUS
MEMORYLESS CHANNEL
DECODING APPARATUS
OUTPUT

FIG.1

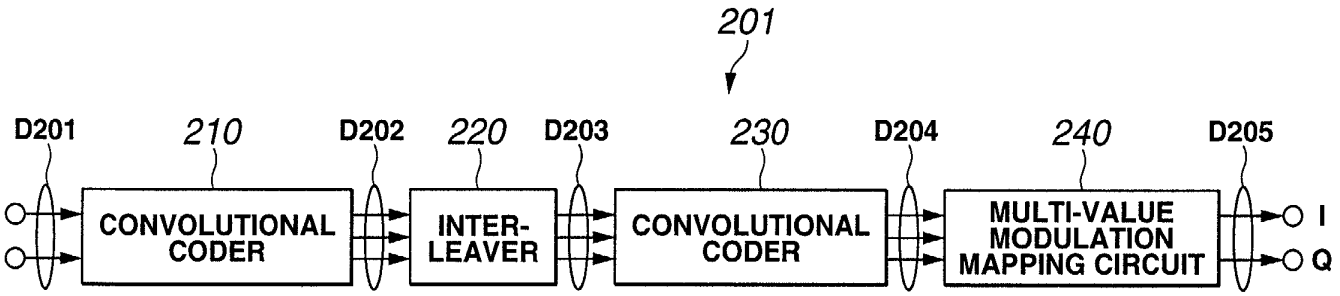
201
D201
210
D202
220
D203
230
D204
240
D205
CONVOLUTIONAL CODER
INTER-LEAVER
CONVOLUTIONAL CODER
MULTI-VALUE MODULATION MAPPING CIRCUIT
I
Q

FIG.2

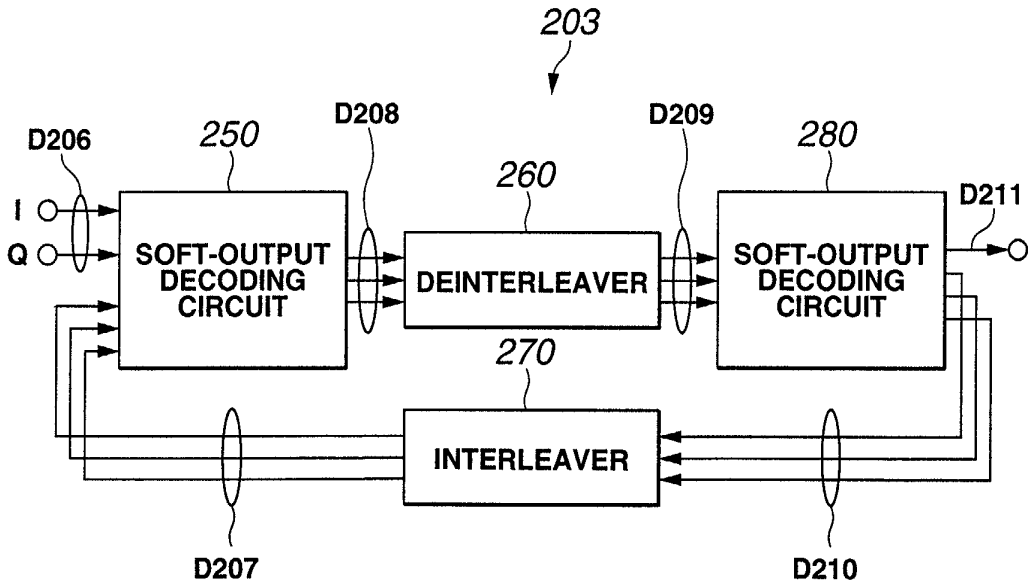
203
D206
250
D208
260
D209
280
D211
I
Q
SOFT-OUTPUT DECODING CIRCUIT
DEINTERLEAVER
SOFT-OUTPUT DECODING CIRCUIT
270
INTERLEAVER
D207
D210

FIG.3

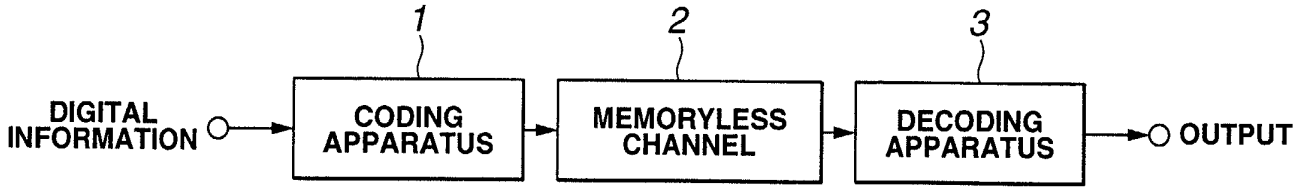

FIG.4

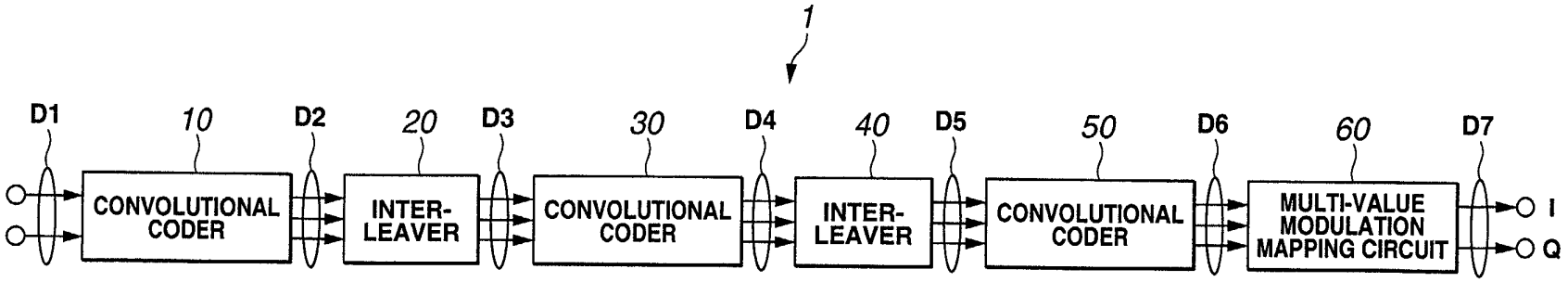

FIG.5

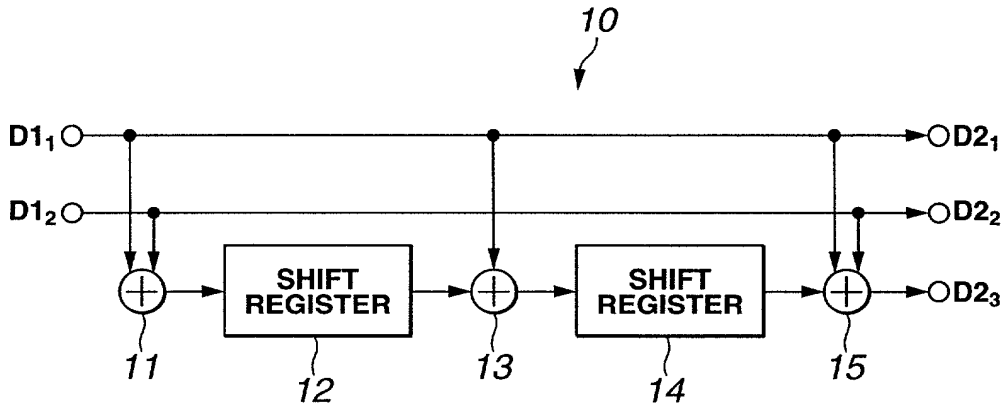
10
D1₁
D1₂
D2₁
D2₂
D2₃
SHIFT REGISTER
SHIFT REGISTER
11
12
13
14
15

FIG.6

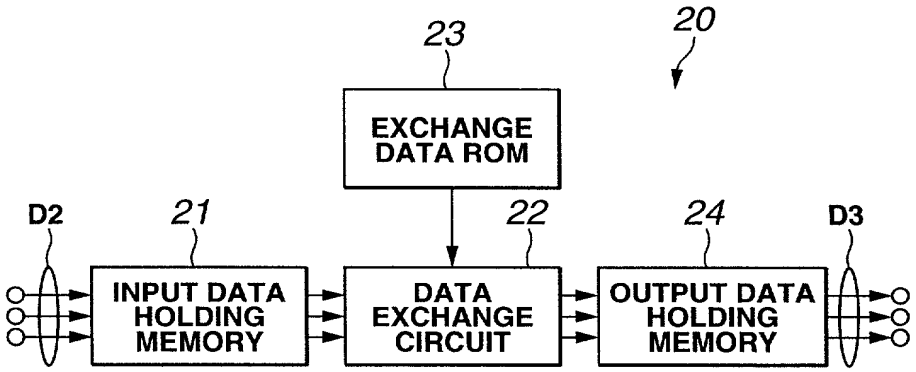
23
20
EXCHANGE DATA ROM
D2
21
22
24
D3
INPUT DATA HOLDING MEMORY
DATA EXCHANGE CIRCUIT
OUTPUT DATA HOLDING MEMORY

FIG.7

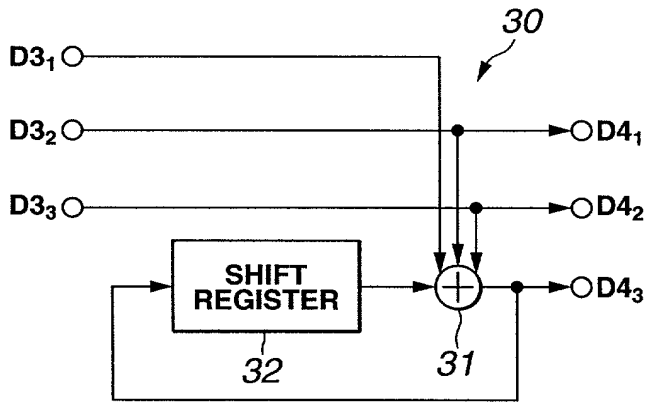

FIG.8

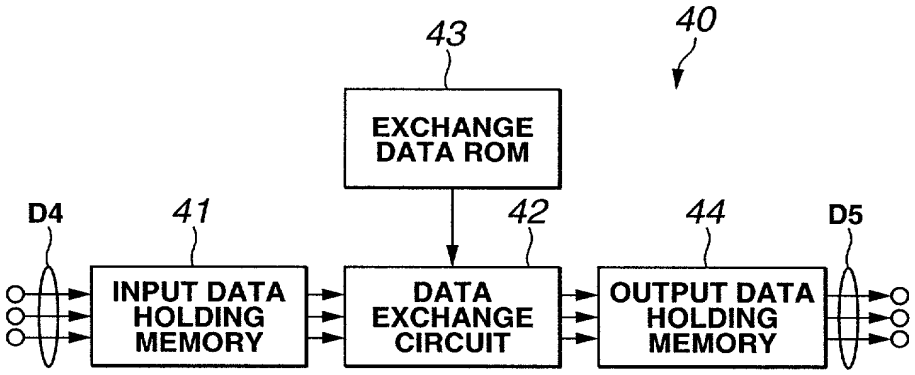

FIG.9

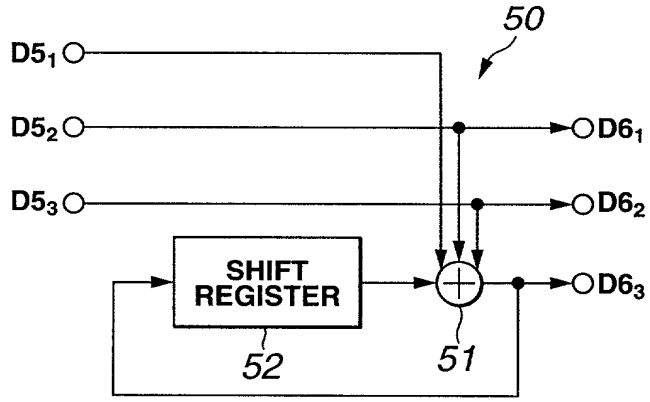

FIG.10

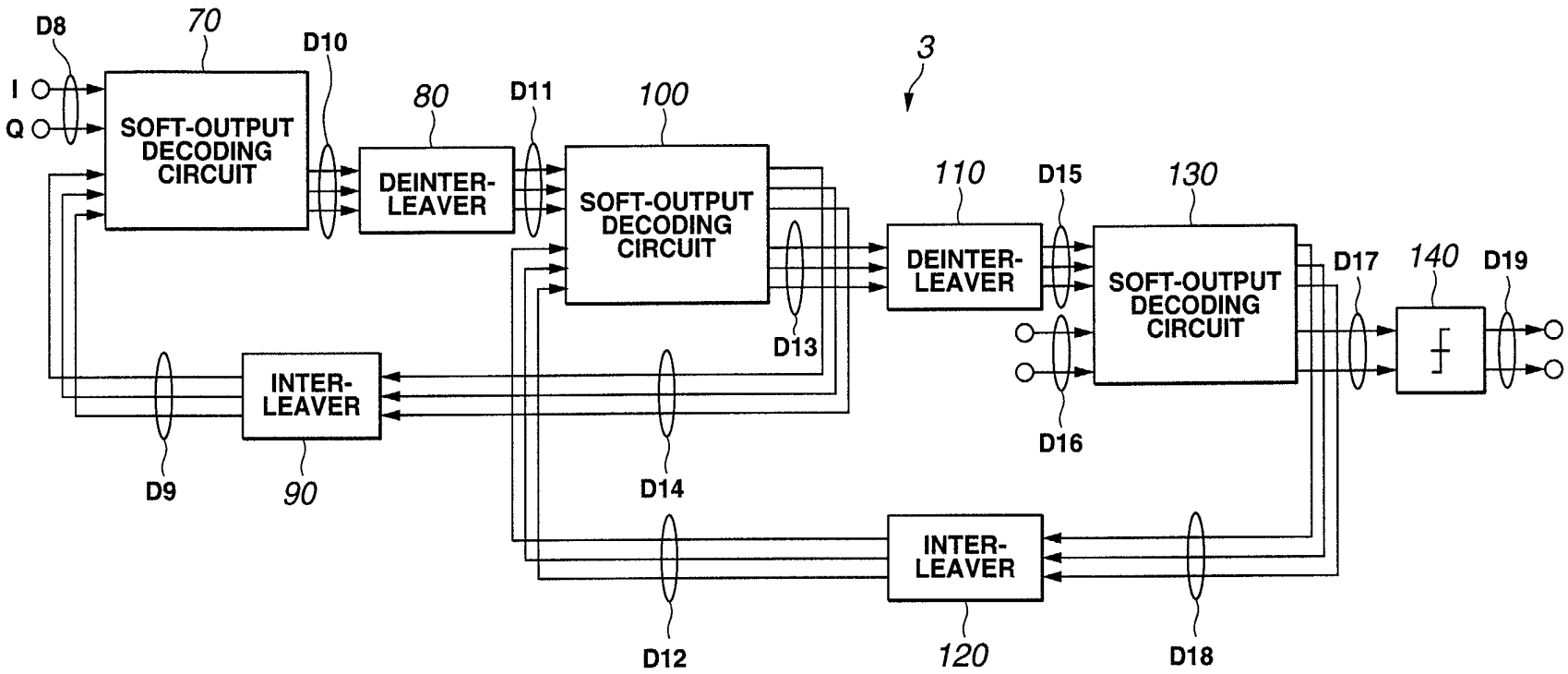

FIG.11

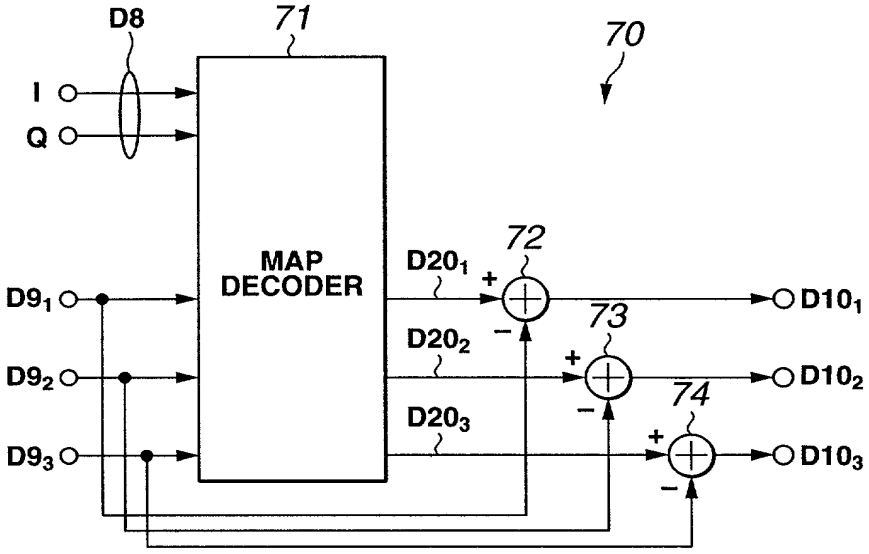
D8
71
70
I
Q
MAP
DECODER
D9$_1$
D9$_2$
D9$_3$
D20$_1$
D20$_2$
D20$_3$
72
73
74
+
−
D10$_1$
D10$_2$
D10$_3$

FIG.12

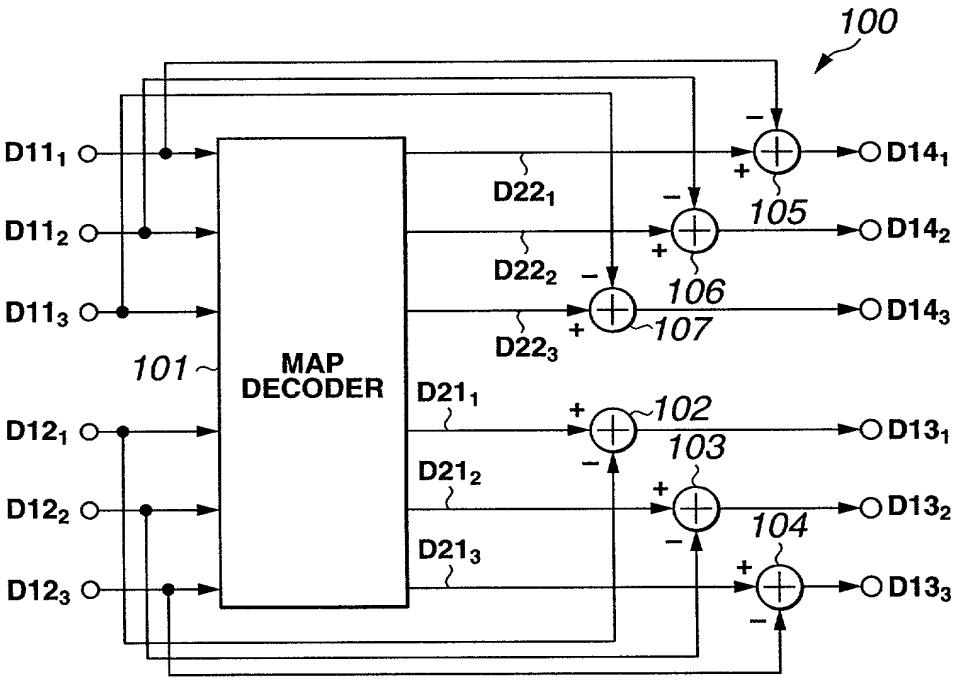
100
D11₁
D11₂
D11₃
101
MAP DECODER
D12₁
D12₂
D12₃
D22₁
D22₂
D22₃
D21₁
D21₂
D21₃
105
106
107
102
103
104
D14₁
D14₂
D14₃
D13₁
D13₂
D13₃

FIG.13

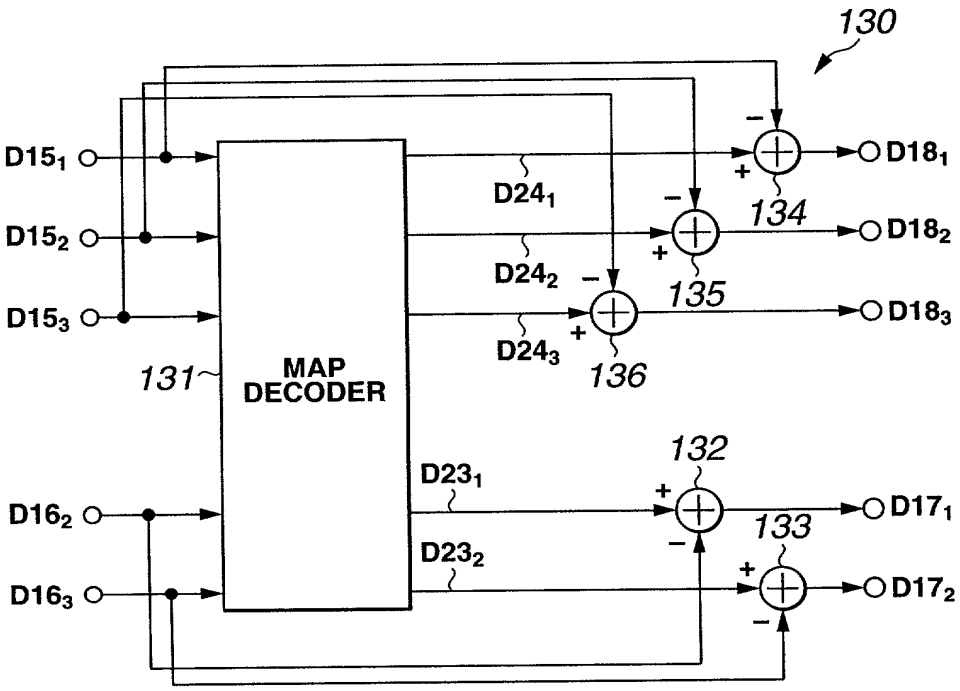
130
D15₁
D15₂
D15₃
131
MAP DECODER
D16₂
D16₃
D24₁
D24₂
D24₃
D23₁
D23₂
134
135
136
132
133
D18₁
D18₂
D18₃
D17₁
D17₂
+
−

FIG.14

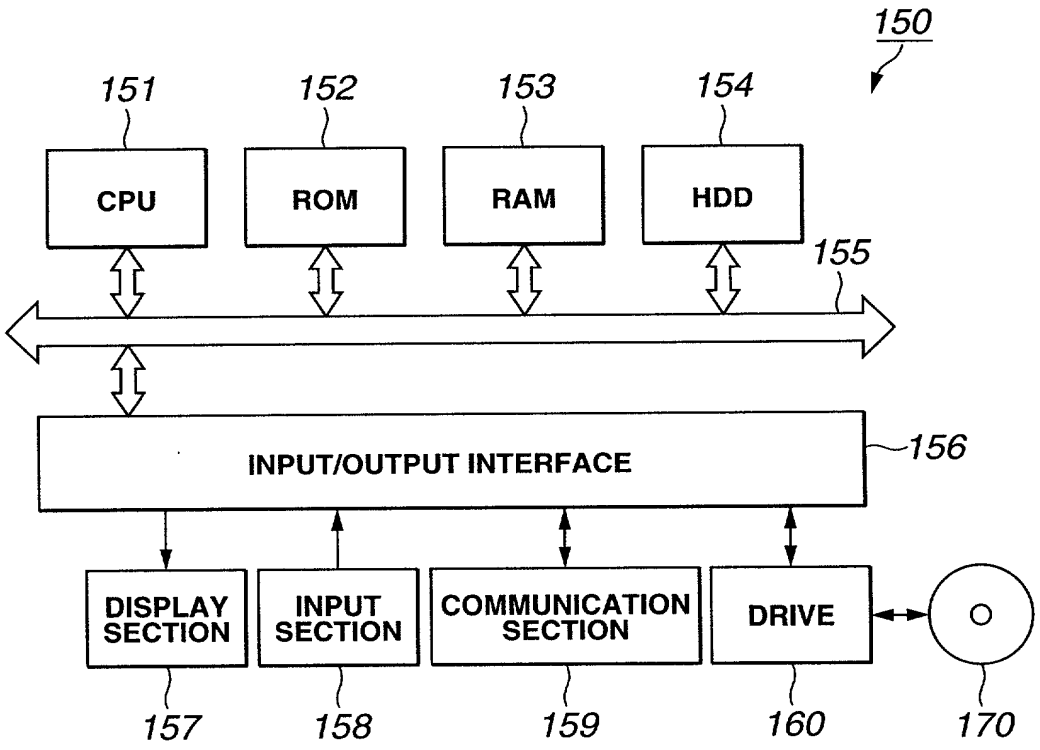
150
151
152
153
154
CPU
ROM
RAM
HDD
155
INPUT/OUTPUT INTERFACE
156
DISPLAY SECTION
INPUT SECTION
COMMUNICATION SECTION
DRIVE
157
158
159
160
170

FIG.15